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TRIMMING OF A TWO POINT PHASE MODULATOR

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TRIMMING OF A TWO POINT PHASE MODULATOR

CROSS REFERENCE TO RELATED APPLICATIONS

This patent application claims priority to, and incorporates herein by reference, U.S. Provisional Application No. 60/478,023, entitled "Trimming of a Two Point Phase Modulator," filed on June 11, 2003. This patent application is a continuation-in-part of U.S. Utility Application No. 10/655,291, entitled "Trimming of a Two Point Phase Modulator," filed on September 4, 2003, and bearing Attorney Docket No. 53807-00072USP1. U.S. Utility Application No. 10/655,291 is a continuation-in-part of U.S. Utility Application No. 10/236,648, entitled "Trimming of a Two Point Phase Modulator," filed on September 6, 2002.

FIELD OF THE INVENTION

The invention relates to direct modulation of a radio frequency signal and, in particular, to direct modulation of a radio frequency signal using a two-point phase modulator.

BACKGROUND OF THE INVENTION

All digital, narrowband radio transmitters that are spectrally efficient require, in principle, two operations to be performed: (1) the baseband data must be filtered to limit the width of its spectrum, and (2) the resulting baseband signal must be translated to the desired radio frequency band. A number of techniques exists for translating the baseband signal to the radio frequency signal. One technique involves feeding the baseband signal directly into the inputs of a frequency synthesizer, such as a PLL (phase-locked loop).

Operation of the PLL is well known to persons having ordinary skill in this field and will therefore not be described here. It will suffice to say that the division factor N of the PLL can be either an integer value or it can be a non-integer value, i.e., a fractional-N PLL. Fractional-N PLLs are usually controlled by sigma delta modulators. The sigma delta modulator switches the division factor of the PLL between different integer values such that the resulting average value of the PLL output signal can be made a fractional multiple of its reference signal.

Applying a baseband signal to the sigma delta modulator results in direct modulation of the fractional-N PLL. Typically, a filtered version of the baseband signal is provided to the sigma delta modulator, which then uses the instantaneous frequency of the baseband signal to vary the frequency division factor of the frequency divider. By controlling the frequency division factor with a sigma-delta modulator, modulation with a constant envelope (i.e., frequency and phase modulation) can be generated. And because the sigma delta modulator takes the place of complicated analog circuitry, extremely compact architectures can be developed for constant envelope systems (e.g., Global System for Mobile Communications (GSM) or Digital Communication Systems (DCS)). Currently, a complete radio transmitter may be integrated into a single ASIC (application specific integrated circuit) using the direct modulation approach.

Constant envelope systems are not bandwidth efficient, however, and therefore some proposed systems also use amplitude modulation in addition to phase and frequency modulation. Examples of these systems include EDGE (Enhanced Data GSM Environment) and WCDMA (Wideband Code Division Multiple Access). In these systems, the modulating signal is divided into a phase part and an amplitude part. The phase part is

introduced in the fractional-N PLL and the amplitude part is added (effectively multiplied) in a post PLL power amplifier. In this way, switching blocks can be used throughout the complete modulator, which is very power efficient.

When dividing the signal into an amplitude and a phase part, however, the respective bandwidth of the phase and of the amplitude part become much wider than that of the combined signal. And since the amplitude and the phase part are combined in a multiplier after the PLL, stringent requirements are imposed on the dynamic range and bandwidth of the amplitude and phase parts, and also on the timing between the amplitude and phase parts.

One way to get around the PLL loop bandwidth limitation is to add another modulation point to the PLL, hence, the term "two-point modulation." In two-point modulation, a second modulation signal is inserted into the PLL after the loop filter. An example of a two-point phase modulator is shown in Figure 1. The two-point phase modulator includes a phase frequency detector 25, a loop filter 65 (which is a low-pass (LP) filter), an adder 11, a voltage controlled oscillator (VCO) 16, a frequency divider 8 in the feedback loop, and a sigma delta modulator 9. A post PLL power amplifier 14 is also present for adding the amplitude part. A similar modulation scheme is described in U.S. Patent No. 5,834,987, entitled "Frequency synthesizer systems and methods for three point modulation with a DC-response," which is incorporated herein by reference.

In operation, the instantaneous frequency f_{inst} of the baseband signal is applied to the PLL 15 at two points: point 10 (at the sigma delta modulator) and point 12 (at the adder). A reference frequency θ_{ref} is applied to the phase frequency detector 25, and an amplitude part

"A" is applied to the power amplifier 14. The transfer function from the modulation inputs to the output of the VCO 16 can be derived as:

$$\theta_{out,VCO}(s) = \frac{f_{inst}(s)}{Ns}\frac{K_{phd}\,K_{vco}/s\;H_{LP}(s)}{1+K_{phd}\,K_{vco}/s\;H_{LP}(s)/N} + \frac{f_{inst}(s)}{K'_{vco}}\frac{K_{vco}/s}{1+K_{phd}\,K_{vco}/s\;H_{LP}(s)/N} = \frac{f_{inst}(s)/s}{1+K_{phd}K_{vco}/s\;H_{LP}(s)/N}\left(K_{vco}/K'_{vco} + K_{phd}\,K_{vco}/s\;H_{LP}(s)/N\right) = \left[If,\ K_{vco} = K'_{vco}\right] = f_{inst}(s)/s \quad (1)$$

As can be seen, the transfer function for the two-point modulator is independent of the PLL loop bandwidth. This eliminates the trade-off between PLL loop bandwidth and modulation bandwidth. Unfortunately, because the transfer function is dependent on the VCO gain, K_{vco}, the scheme results in a new unknown being introduced, namely, the estimation of the VCO gain, K'_{vco}. If K'_{vco} is wrong, then spectral growth may result that may compromise the ACPR (adjacent channel power ratio) requirement of the system.

A standard VCO configuration is depicted in Figure 2. As can be seen, the VCO includes a resonator composed of inductors L1, L2 (20, 22) and varactors C_v (30, 32). Parasitic capacitance C_{par} (24) represents all capacitor loading and all parasitic capacitances as seen from the resonator. Also present is a tuning network composed of coupling capacitors C_c (26, 28) and R_{gnd} (34, 36) (ground reference for the varactors) for coupling the varactors C_v loosely to the resonator. The bottom part of Figure 2 shows the active components (e.g., transistors 38, 40) responsible for sustaining the oscillation. In a radio

frequency (RF) ASIC with an onboard VCO, the VCO gain is dependent on the size of the inductor, the output frequency, and the bias point of the varactor.

The tuning sensitivity (VCO gain) of the VCO is derived by taking the derivative of the VCO center frequency w_o with respect to the tuning voltage, as follows:

$$w_o = \frac{1}{\sqrt{L_{tot}C_{tot}}};$$

$$\frac{\partial w_o}{\partial V_{tune}} = \frac{\partial w_o}{\partial C_{tot}} \frac{\partial C_{tot}}{\partial C_V} \frac{\partial C_V}{\partial V_{tune}} = -\frac{L_{tot}}{2(L_{tot}C_{tot})^{3/2}} \frac{1}{2}\left(\frac{C_c}{C_c + C_V}\right)^2 \frac{\partial C_V}{\partial V_{tune}} = \quad (2)$$

$$-\frac{L_{tot}w_o^3}{2} \frac{1}{2}\left(\frac{C_c}{C_c + C_V}\right)^2 \frac{\partial C_V}{\partial V_{tune}}$$

As can be seen from Equation (2), the tuning sensitivity is dependent on many parameters. For example, the VCO on-chip inductors (e.g., L1, L2) is a large metal structure and is inherently stable. The varactor capacitance and the slope of the varactor capacitance are dependent on the tuning voltage V_{tune} (42). The tuning voltage V_{tune}, in turn, is dependent on the VCO center frequency. By making a careful design and keeping the above equation in mind, however, the total VCO gain variation can be reduced.

A table with measured VCO gain versus frequency can compensate for variations in the VCO gain. The main problem with this solution, however, is that when manufacturing the circuits, the parasitic capacitance (C_{par}) of the resonator varies, and therefore a different tuning voltage is required to get the correct output frequency. The VCO gain may vary as much as 50% from one sample to another. This means that the VCO gain would have to be measured for each VCO chip to get stable performance.

An alternative solution is described in U.S. Patent No. 5,834,987, which is a modified VCO circuit configuration where the VCO has two separate inputs, one for the PLL tuning voltage and one for the modulation input. This type of circuit configuration is

depicted in Figure 3. As can be seen, the circuit of Figure 3 is similar to the circuit of Figure 2 except that a separate tuning input V_{mod} (50) and modulation varactors C_{V1} (30-1, 32-1) are added for modulation. Coupling capacitors C_{C1} (26-1, 28-1), and grounding resistors R_{gnd1} (34-1, 36-1) are also present. The V_{mod} tuning input is similar to the V_{tune} tuning input (42), but has a DC voltage applied to set the operating point of the varactors C_{V1}. This allows the modulation varactors C_{V1} to be biased at a suitable DC level. Also, the input bandwidth and tuning sensitivity can be optimized for modulation. If the DC level applied to the varactors C_{V1} is constant, the only thing varying in Equation (2) is the center frequency. In other words, the modified VCO solution is independent of parasitic capacitor variations, since such variations are compensated in the tuning voltage. This means that the VCO gain variation from sample to sample is mainly dependent on spread in the varactor at the specific bias point and spread in the coupling capacitor. But by careful design, the VCO gain variation can be made less than 10% (mainly by choosing large size components).

Although the above described designs have merit, they may not be sufficient for some systems with strict requirements for VCO gain estimation, such as EDGE and WCDMA systems. Moreover, for future systems with more complex modulation schemes (e.g., 16QAM), the requirement of VCO gain estimations will be even higher. Therefore, some kind of automatic calibration or trimming of the VCO gain is needed.

BRIEF SUMMARY OF THE INVENTION

The present invention is directed to a method and system for automated calibration of the VCO gain in phase modulators. The method and system of the invention comprises synthesizing, in a phase modulator, a signal having a given output frequency using a

controlled oscillator having a frequency control input, a modulation input, and a feedback loop. A frequency control signal is applied to the frequency control input, and gain variation of the controlled oscillator is compensated for outside of the feedback loop via the modulation input. The method and system of the invention may be employed in any telecommunication system that uses phase and amplitude modulation, including EDGE and WCDMA systems.

In general, in one aspect, the invention is directed to a phase modulator. The phase modulator comprises a phase-locked loop having a phase frequency detector, a low-pass modulation input coupled to the phase frequency detector, a voltage controlled oscillator, and a high-pass modulation input coupled to the voltage controlled oscillator. A trimming circuit is connected between the phase frequency detector and the voltage controlled oscillator. The trimming circuit is configured to receive an error signal from the phase frequency detector and to control a gain of the high-pass modulation input such that the high-pass modulation input and the low-pass modulation input together form an all-pass modulation input to the voltage controlled oscillator.

In general, in another aspect, the invention is directed to a method of a controlling a gain of a voltage controlled oscillator in a phase modulator having a phase-locked loop that includes a phase frequency detector, a low-pass modulation input coupled to the phase frequency detector, the voltage controlled oscillator, a high-pass modulation input coupled to the voltage controlled oscillator, and a trimming circuit. The method comprises the steps of receiving an error signal from the phase frequency detector in the trimming circuit, and controlling a gain of the high-pass modulation input using the trimming circuit and the error

signal such that the high-pass modulation input and the low-pass modulation input together form an all-pass modulation input to the voltage controlled oscillator.

In general, in yet another aspect, the invention is directed to a phase-locked loop. The phase-locked loop comprises a phase frequency detector, a voltage controlled oscillator, and a trimming circuit connected between the phase frequency detector and the voltage controlled oscillator. The trimming circuit is configured to receive an error signal from the phase frequency detector and to control a gain of the voltage controlled oscillator based on the error signal and an estimation of the gain of the voltage controlled oscillator.

In general, in still another aspect, the invention is directed to a frequency synthesizer. The frequency synthesizer comprises a voltage controlled oscillator having a tuning input which is responsive to a frequency control input signal to generate an output frequency, and having a feedback loop, and a compensation circuit for compensating gain variation of the controlled oscillator outside of the feedback loop.

It should be emphasized that the term comprises/comprising, when used in this specification, is taken to specify the presence of stated features, integers, steps, or components, but does not preclude the presence or addition of one or more other features, integers, steps, components, or groups thereof.

BRIEF DESCRIPTION OF THE DRAWINGS

A better understanding of the invention may be had by reference to the following detailed description when taken in conjunction with the accompanying drawings, wherein:

Figure 1, previously described in part, is a block diagram showing two-point modulation;

Figure 2, previously described in part, is a simplified schematic of a typical differential, on-chip VCO;

Figure 3, previously described in part, is a simplified schematic of a modified VCO optimized for modulation;

Figure 4 is a block diagram showing a modified phase frequency detector with an extra charge pump according to embodiments of the invention;

Figure 5 is a block diagram of a modulator using two-point phase modulation and feedback for setting the VCO gain estimation according to embodiments of the invention;

Figure 6 is a block diagram of another embodiment of a modulator using two-point phase modulation and feedback for setting the VCO gain estimation according to embodiments of the invention;

Figure 7 is a block diagram of a modulator similar to Figure 6, modified to measure the loop voltage instead of the charge pump output according to embodiments of the invention;

Figure 8 is a block diagram of another modulator modified to measure the loop voltage instead of the charge pump output according to embodiments of the invention;

Figure 9 is a block diagram of an exemplary implementation of a loop voltage amplifier for the modulator of Figure 8;

Figure 10 is a schematic diagram of an exemplary implementation of the VCO trimming loop for the modulator of Figure 8;

Figure 11 is a schematic diagram of an exemplary implementation of the loop voltage amplifier shown in Figure 8;

Figure 12 is a schematic diagram of an exemplary implementation of the limit/delay block shown in Figure 8;

Figure 13 is a schematic diagram of an exemplary implementation of the mixer shown in Figure 8; and

Figure 14 is a schematic diagram of an exemplary implementation of the variable gain block shown in Figure 8.

DETAILED DESCRIPTION OF PREFERRED EXEMPLARY EMBODIMENTS OF THE INVENTION

Following is a detailed description of embodiments of the invention with reference to the drawings wherein numerals and labels for similar elements are carried forward.

As mentioned previously, certain systems such as EDGE and WCDMA as well as future systems with more complex modulation schemes (for example, 16QAM) require more stringent VCO gain estimations using the modulation scheme described above. Accordingly, the present invention is directed to a method and system for automatic calibration of the VCO gain. Also, using automatic calibration may result in a higher yield on the fabrication side and more stable operation.

Referring again to the modified VCO of Figure 3, compensation for VCO gain variations can be applied by changing the DC level at the modulation input varactors C_{V1}. By applying the VCO gain estimation K'_{VCO} after the digital-to-analog converter (DAC) (not expressly shown), which is used for applying the modulation at the VCO input (i.e., point 12 of Figure 1), the dynamic range requirement of the DAC is not affected. These general considerations apply for the below-described feedback systems as well.

Referring back to the two-point modulator of Figure 1, the modulation signal applied at the VCO input (point 12) causes a change in the VCO output frequency. As a result, a counteracting output is produced by the phase frequency detector 25 to try and correct the VCO output frequency. When the same modulation signal is applied at the pre-scaler (i.e., frequency divider) 8 input, however, the error signal from the phase frequency detector output is zero. The scheme in Figure 1 results in the following transfer function for the phase frequency detector 25:

$$\theta_{out,PFD}(s) = f_{inst}(s)\frac{K'_{vco} - K_{vco}}{K'_{vco}}\frac{\frac{K_{phd}}{Ns}}{1+\frac{K_{phd}K_{vco}H_{LP}(s)}{Ns}} \qquad (3)$$

As can be seen from Equation (3), the output from the phase frequency detector can be used to trim the VCO gain estimation. For example, in some embodiments of the invention, an extra charge pump may be added to the phase frequency detector in parallel to the presently existing charge pump. Figure 4 shows an exemplary implementation of a phase frequency detector 80 according to embodiments of the invention. The phase frequency detector 80 is similar to conventional phase frequency detectors in that the reference signal and the pre-scaler (frequency divider) signal are provided to flip-flops 406 and 408, respectively. The flip-flops 406 and 408 control a charge pump 402, causing it to output a charge proportional to the phase difference between the reference and pre-scaler inputs. An AND-gate 410 is used for resetting the flip-flops and the delay cell 412 is used for deadband compensation.

In accordance with embodiments of the invention, the phase frequency detector 80 includes a second charge pump 404 connected in parallel with the first charge pump 402 as shown. The two charge pumps produce two error signals, namely, output currents 60 and

62, with about the same duty cycle. The first output 60 is used for the PLL loop filter as is commonly done in the art, while the second output 62 provides feedback to the VCO for trimming the VCO gain estimation.

Figure 5 illustrates an exemplary two-point phase modulator 500 using the phase frequency detector 80 according to embodiments of the invention. The scheme in Figure 5 is similar to the scheme in Figure 4 in that the first error signal 60 is provided to the loop filter 65. The modulator 500 includes a trimming or control loop that comprises a matched filter 70 and a variable gain amplifier 75. The second error signal 62 from the second charge pump 404 is then provided to the matched filter 70, which is used for measuring the modulation error due to VCO gain estimation error and also sets the dynamics of the regulation (e.g., the settling time and the ringing during settling) of the trimming loop. The filter 70 should be able to detect the polarity of the error signal 62 to produce the correction signal. This polarity can be measured by correlating the error signal 62 with the original modulation signal f_{inst}.

Figure 6 illustrates another embodiment of the two-point phase modulator 600 in which compensation for VCO gain variation due to center frequency variations is added. The modulator 600 of Figure 6 is similar to the modulator 500 of Figure 5, except that a variable gain amplifier 175 has been added as the input of the second modulation signal. This allows a rough estimation of the VCO gain variation (based on the center frequency w_0) from the DAC (not expressly shown) to be used, which reduces the gain range of the feedback path. Also, the adder 11 has been removed and a VCO 116 with a separate modulation input 90 has been added. Using this VCO 116, the amplifiers 75 and 175 can be employed to change the DC level applied to the varactors (see Figure 3). Because the

frequency dependent part (see Equation (2)) of the VCO gain variation is known, it may be compensated for outside the feedback loop. Compensating for part of the VCO gain estimation error outside the feedback loop enables a shorter settling time, since the range of the variable amplifier 75 in the control loop may be reduced because the initial error is smaller.

In one exemplary implementation of the above scheme, a small test signal can be applied to the two modulation points. If the VCO gain estimation is correct, there will be no output from the phase frequency detector 80. Otherwise, if the integrated PLL output signal is sampled coherently at the test signal frequency, a DC voltage corresponding to the mismatch results. This voltage can be used to set the gain in the second modulation path including the amplifiers 175, 75. The result is a feedback system for controlling the VCO gain estimation. Some additional filtering (e.g., via the matched filter 70) can be applied to get the correct dynamics in the compensation loop.

The test signal appears at the PLL output and, therefore, has to be chosen low enough not to destroy the adjacent channel power ratio (ACPR) spectra when it is applied outside the transmit channel, or the EVM (error vector magnitude) when the signal is applied inside the transmit channel. The test signal is mixed with the amplitude signal after the PLL (see Figure 1) so it will not appear as a spur at the modulator output.

Also, when using the dual charge pump solution, the error signal measured represents a high pass (HP) filtered version of the phase error signal. Since the main energy of the error signal is contained in the low frequency (LF) part, this may mean the quality of the error signal is less than optimal.

If the error signal is measured after the loop filter instead, then a low-pass (LP) filtered version of the frequency error results, which may be used for automatic tuning. The error signal then becomes:

$$f_{error}(s) = f_{inst}(s)\frac{K'_{vco} - K_{vco}}{K'_{vco}}\frac{\frac{K_{phd}H_{LP}(s)}{Ns}}{1+\frac{K_{phd}K_{vco}H_{LP}(s)}{Ns}} \quad (4)$$

This requires that both frequency insertion points are DC coupled. A block diagram of this solution is presented in Figure 7. As can be seen, the modulator 700 of Figure 7 is different from the modulator 600 of Figure 6 in that the matched filter 70 has been relocated to after the loop filter 65. This allows the loop voltage to be measured and used to control the VCO gain.

Figure 8 shows another two-point phase modulator 800 which uses the loop voltage to control the VCO gain according to some embodiments of the invention. The two-point phase modulator 800 includes all of the components of the modulator 700 shown in Figure 7. In addition, the two-point phase modulator 800 also includes a loop voltage amplifier 802, a limit/delay block 804, and a mixer 806. A signal "Trimstart" is used to initiate the gain trimming process and is triggered within a certain amount of time after the PLL begins its phase locking process. To trim the VCO gain, an error signal 810 is measured in the loop after the loop filter 65, but before the adder 11. The error signal 810 is then amplified and filtered by the loop voltage amplifier 802, then mixed in the mixer 806 with a delayed/limited version of the modulation signal. An integrator 808 integrates the mixed signal from the mixer 806, and a variable gain amplifier 75 adjusts the gain of the VCO modulation signal prior to its combination with the error signal 810 via the adder 11. A second variable gain amplifier 175 allows a rough estimation of the VCO gain variation due

to the center frequency w_0 to be used, which reduces the gain range of the feedback path. As mentioned above, the amplifiers 75 and 175 can be used to change the DC level applied to the varactors (see Figure 3). An exemplary implementation of each of these blocks will now be described.

Figure 9 illustrates an exemplary implementation of the loop voltage amplifier 802. The purpose of this amplifier is to amplify the error signal 810 so that it is less constrained by the matching and noise requirements of the subsequent circuitry in the modulator. The error signal 810 is inversely proportional to the VCO gain. Assuming a maximum VCO gain of 60 MHz/V and an average frequency deviation of 60 kHz, the signal level at the VCO input will be about 1 mV. Assuming further that the maximum residual error is about 5 percent, the minimum level for the error signal 310 will be about 50 μV. Since the loop voltage may vary by as much as 2V, depending on the transmitter output frequency and parameters spread, the dynamic range requirement of the modulator becomes greater than 90dB (20log(2V/50μV) = 92dB).

Also, since the loop voltage is a DC component, it may be removed by a high pass filter inserted before the amplifier 902. Mobile telephone systems such as GSM (Global System for Mobile Communication) and EDGE (Enhanced Data GSM Environment), however, are based on TDMA (Time Division Multiple Access), for which there is a transient in the loop voltage for every slot due to the PLL locking. But this may be overcome by implementing a feedback amplifier with a variable high pass cut off frequency. Then, during PLL locking, the cut off frequency is high, and after the PLL is locked, the gain trimming loop is activated by Trimstart, which lowers the high pass filter cut off frequency.

In an exemplary implementation, the PLL locking time may be about 75 μS. The Trimstart signal is triggered after this time using, for example, a counter, to start the gain trimming process. The gain trimming loop settling time may also be on the order of 75 μS, which results in a total calibration time of about 150 μS, a value that is sufficient for GSM/EDGE systems.

In Figure 9, V_{loop} represents the error signal 810. A low pass filter 900 suppresses any high frequency noise from the error signal 810. Such high frequency noise may result from peaking and group delay ripple at the PLL loop bandwidth. The cut off frequency of the low pass filter should be lower than the PLL loop bandwidth. For example, if the PLL 3 dB loop bandwidth is 150 kHz, the low pass filter cut off frequency should be about 60 kHz.

The output of the low pass filter is provided to a differential amplifier 902. In some embodiments, the differential amplifier 902 has a gain of about 20. The output of the differential amplifier 902 is provided to a transconductance cell 904. For a bipolar transistor, the transconductance is defined as:

$$g_m = \frac{\partial i_c}{\partial v_{be}}, v_{cb} = 0 \qquad (5)$$

where i_c is the collector current, v_{be} is the base-emitter voltage, and v_{cb} is the collector-base voltage. The output of the transconductance cell 904 is then provided to the mixer 806.

The output of the differential amplifier 902 is also provided to a second transconductance cell 906. The transconductance value of this cell 906 may be used to set the bandwidth of the amplifier 802 (the amplifier 802 has high pass characteristics that combine with the low pass filter 900 to form a bandpass filter) as follows:

$$V_{FB} = \frac{V_{in}}{1 + s\frac{C}{A \cdot g_m}} \tag{6}$$

Before receiving the Trimstart signal, the transconductance value of the transconductance cell 906 is about 200 μA/V, the capacitance C is about 500 pF, and the differential amplifier gain is about 20, which translates to a 3dB bandwidth of about 1.3 MHz. Note that the step response is slew-rate limited in this case, with the slew-rate limit defined as:

$$\frac{\Delta V}{\Delta I} = \frac{I}{C} = \frac{11\mu A}{500 pF} = 22kV/s \tag{7}$$

Thus, based on the slew-rate limit, a 1 V step would take about 45 μS.

After the Trimstart signal is received, the transconductance value of the cell 906 becomes 1μA/V, and the 3dB bandwidth becomes 60 kHz. Hence, the loop voltage amplifier 802 is now a bandpass amplifier with a bandwidth of about 6-60 kHz.

As for the mixer 806, referring back to Figure 8, this component is used to correlate the original input signal f_{inst} with the error signal 810 to arrive at the proper sign for the feedback signal. In some embodiments, an ordinary Gilbert mixer may be used to implement the mixer 806.

The limit/delay block 804 allows the mixer 806 to work correctly by compensating for the group delay of the PLL. In some embodiments of the invention, the limit/delay block 804 may be implemented by switching in/out one or more RC networks.

The integrator 808 is used to integrate the output from the mixer 806. The average output signal of the mixer 806 is a voltage corresponding to the error in the VCO gain setting. In some embodiments of the invention, this voltage is converted into a current in a

transconductance cell of the integrator 808, then integrated by a capacitor of the integrator 808. The voltage across this capacitor is then used to control the gain of the amplifier 75. In some embodiments, the transconductance of the integrator 808 may be programmable in order to optimize the loop settling time. In any case, since the error signal 810 is inversely proportional to the VCO gain, the transconductance should be proportional to the VCO gain.

Figure 10 is a top-level schematic of an exemplary implementation of the VCO trimming loop shown in Figure 8. In Figure 10, the lower left portion represents the loop voltage amplifier 802, the upper left portion represents the limit/delay block 804, the middle section represents a combination of the mixer 806 and the transconductance cell 808, and the right portion represents the variable gain amplifiers 75 and 175. The signals labeled "f_mom" and "f_mom_bar" represent the differential versions of f_{inst}/K'_{VCO}, and "LOn" and "LOp" represent the delayed and limited versions of f_mom and f_mom_bar, respectively. Imixern and Imixerp represent the differential output currents from the differential amplifier 802 that goes into the mixer 806. "Sbt" represents the connection to the on-chip substrate. "Vfb" represents the feedback node in the differential amplifier 802, and "Vbgr" represents a reference voltage from an on-chip band-gap reference that sets the bias point for the entire circuit. "Vcc" and "Gnd" represent the supply voltage and ground, respectively. An exemplary implementation of each of these blocks is described below.

Referring now to Figure 11, an exemplary implementation of the loop voltage amplifier 802 of Figure 9 is shown. In this figure, R0 and C2 provide an exemplary implementation of the low pass filter 900. M1, M2, R21, and R22 provide an exemplary implementation of the differential amplifier 902. Q2 and Q3 are used for voltage level shifting. Q17, R15, and M3-M6 are used to set the DC bias point. Q4 and Q5 provide the

transconductance that drives the mixer (DC biased by Q18 and R5). Q12-Q15, Q6, Q7, Q26, and Q27 provide the transconductance that drives the feedback path. C7 is the integrating capacitor. The transconductance is switchable by connecting Q20, R8, M7 or Q19, R23, M0 using the Trimstart signal.

Figure 12 illustrates an exemplary implementation of the limit/delay block 804. In this figure, Q18, Q19, R18, and R19 provide the limiter, and the RC combination R18, R20, and C1, C2 provide the delay. The bias point is set by Q17 and R15.

Figure 13 illustrates an exemplary implementation of the mixer 806. In this figure, Q6-Q9 provide a standard Gilbert mixer and R1 and R2 are the mixer load resistors. Q22 and Q23 (DC biased by Q23, Q26 and R9, R11) are used for DC level shifting. The transconductance driving the integrating capacitor C1 is formed by Q3, Q4, Q10, and Q11 (DC biased by Q25 and R0). The voltage across C1 then controls the gain of the frequency path.

Figure 14 illustrates an exemplary implementation of the variable gain amplifiers 75 and 175. This block converts the differential frequency signal to a single-ended one that can drive V_{mod} (see Figure 3). The voltage across resistor R34 modulates V_{mod} of the VCO. Transistors M3 and M4 form a current mirror. Transistor Q35 and resistor R44 are used to set a DC-current/voltage through resistor R34. This allows the frequency input to be negative. Transistors Q18 Q19, M1, and M2 together with resistors R43 form an emitter degenerated transconductance (DC biased by transistors Q32 and Q33 and resistors R40 and R41) that outputs a current to the current mirror formed by transistors M3 and M4. This circuitry forms the fixed gain part.

The variable gain part is formed by another transconductance that is made up of transistors Q12, Q13, M1, and M2 and resistor R42 (DC biased by transistors Q30 and Q31 resistors R38 and R39). To allow gain variations, a Gilbert gain amplifier is formed with transistors Q14-Q17, Q36 and Q37. The Gilbert gain amplifier is current controlled using the transconductance formed by transistors M23 and M24 and resistor R18 (DC-biased by transistors Q27 and Q28 and resistors R15 and R16).

The gate DC level of transistor M24 is set by transistor Q29 and resistor R17, R45 and transistor Q0. Prior to the Trimstart signal (i.e., during PLL locking), the variable gain part is set to half the maximum value using the MOS switch M10. This allows the gain to vary symmetrically downward and upward after the Trimstart signal is issued.

Embodiments of the invention have been described above with reference to the two modulation points, at the VCO and the frequency divider input. The invention, however, may be equally applied to any two-point modulator which has one low pass path and one high pass path. For instance, the low pass path may be supplied through the PLL reference signal.

While particular embodiments and applications of the present invention have been illustrated and described, it is to be understood that the invention is not limited to the precise construction and compositions disclosed herein and that various modifications, changes, and variations may be apparent from the foregoing descriptions without departing from the spirit and scope of the invention as defined in the appended claims.